Design of a Low Power and Wide Frequency Range Ring VCO

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Abstract: This paper proposes a low-power, wide frequency range ring VCO circuit structure based on the application of switch power supply modulation technology. Circuit simulation is completed based on CMSC 180nm BCD process. Simulation results show that the VCO circuit can work at a power supply voltage of 3-5 V, and it has a relatively wide frequency range. Under a 5V power supply voltage and a control voltage range of 4.2V~2.2V, the output frequency range is 0.4-11.96MHz. Under a 3V power supply voltage and a control voltage of 2.2V~0.2V, the output frequency range is 0.56~12.3MHz. For the VCO circuit, the maximum average working current of the power supply is less than 80uA, and the average current of the power supply is only 35uA under a 5V power supply voltage and a 10MHz working frequency. The VCO circuit meets the requirements of low power consumption. It can be applied to switch power supply chips.

Keywords: Ring VCO; Voltage Controlled Current Source; Wide Frequency Range; Low Power

1. Introduction

Oscillator circuits are commonly used module circuits in power supplies and high-voltage analog integrated circuits. There are three main control technologies for switching power supplies: Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM), and Pulse Width Frequency Modulation (PWM-PFM). PWM controls the output using the pulse width, while PFM controls the output using the presence or absence of pulses [1]. In modern power integrated circuits, on-chip integrated Voltage-Controlled Oscillator (VCO) circuits typically generate clock signals to modulate switching power supplies. Particularly in PFM modulation mode, the clock frequency needs to change with the voltage. VCO circuits can be divided into ring VCO circuits and LC-VCO circuits. LC-VCO circuits have advantages such as low phase noise and large output swing, but they have a narrow output frequency range and include inductor components, resulting in a larger on-chip integration area. In contrast, ring VCO circuits offer benefits like low power consumption, a wide output frequency range, small area, and ease of integration, which make them widely used [2]. In recent years, research on ring VCOs has focused on low power consumption, low phase noise, a wide frequency range, and high linearity [3-6]. References [3,4,6] propose various differential ring VCO circuits that optimize phase noise performance and have higher common-mode interference rejection capabilities. However, these circuits are complex, and compared to single-ended ring VCO circuits, they significantly increase power consumption and chip area. In the low-frequency switching power supply field with switching frequencies between 1-10MHz [7-9], single-ended ring VCO circuits are the optimal choice. The current-starved ring VCO structure, due to its low sensitivity to PVT (Process, Voltage, and Temperature) variations, is currently widely used in many fields. Reference [10] proposes a three-stage current-starved ring oscillator structure based on an additive current source, reducing the standard deviation by 65.1%.

This paper proposes a low power, wide-frequency-range current-starved ring VCO circuit structure based on the CMSC 180nm BCD process, suitable for use in PFM controllers. The operating voltage range is 3-5V, achieving a maximum input-output relationship K of 5.8MHz/V within a 2V control voltage variation range. At a supply

voltage of 5V and an operating frequency of 10MHz, the average operating current is 35μA. The feasibility of the circuit structure has been verified through circuit simulation.

2. Circuit Design

The traditional ring oscillator structure, as shown in Figure 1, employs an odd number of inverter stages. If the delay time of each inverter is tpd, the oscillation period of a ring oscillator composed of n inverters is $2nt_{pd}$, the delay time tpd can be adjusted by changing the driving current and the equivalent capacitance of the inverters, thereby controlling the frequency of the ring oscillator. However, the delay time of inverters is very short, making the traditional ring oscillator structure impractical, as the oscillation frequency is difficult to adjust. The ring VCO circuit, on the other hand, includes a function to control the output oscillation frequency. The relationship between the frequency of a voltage-controlled oscillator (VCO) and the input control voltage is given by Equation (1), where ω is the output frequency of the VCO, ω_0 is the free frequency, and K i represents the VCO gain, indicating the input-output relationship.

$$\omega = \omega_0 + KV_{in} \quad (1)$$

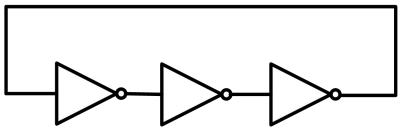


Figure 1. Traditional Ring Oscillator Circuit Structure

2.1 Designed Ring VCO Circuit Structure

The block diagram of the ring VCO circuit proposed in this paper is shown in Figure 2. It includes a bias signal generation circuit, a base current source I0, an input voltage controlled current source source Iv, a delay control inverter composed of PMOS transistor M2 and NMOS transistor M1, a delay capacitor C1, a Schmitt trigger S1, an odd-numbered inverter chain consisting of inverter Inv1, inverter Inv2, and inverter Inv3, and an output buffer Buf1. In Figure 2, the delay control inverter, Schmitt trigger, and odd-numbered inverter chain are cascaded to form an odd-numbered ring oscillator circuit with a total of 5 stages, generating an oscillating clock signal.

The value of delay capacitor C1 is much larger than the equivalent capacitance of the inverter, meaning that the frequency variation of the oscillator output clock signal OSC is controlled by the charging and discharging of delay capacitor C1 through the delay control inverter driven by the voltage controlled current source. The total voltage controlled current source Ic consists of two parts: the reference current source I0 and the input voltage controlled current source Iv. I0 is directly controlled by the output voltage Vbp of the bandgap reference circuit to generate a fixed frequency, while Iv is controlled by the input control voltage Vin. When Vin decreases, the current of the input voltage controlled current source Iv increases, causing the total voltage controlled current source Ic to increase, reducing the charging time of delay capacitor C1, and thus increasing the frequency of the clock signal OSC. Conversely, when Vin increases, the current of the input voltage controlled current source Iv decreases, reducing the total voltage controlled current source Ic, increasing the charging time of delay capacitor C1, and consequently decreasing the frequency of the clock signal OSC.

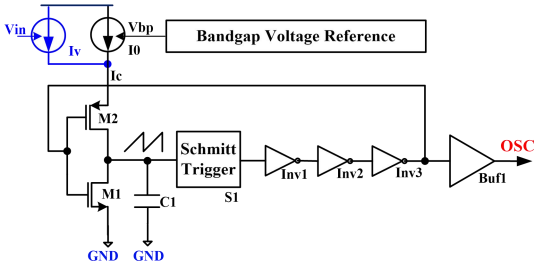


Figure 2. Schematic Block Diagram of VCO Circuit of this Design

In Figure 2, the triangular waveform is obtained at the terminal of delay capacitor C1. To obtain a square wave signal, a Schmitt trigger is used instead of the second inverter after the first stage delay control inverter. The hysteresis characteristic of the Schmitt trigger makes it widely used in shaping circuits, while effectively suppressing noise in the circuit and improving the circuit's anti-interference ability. The paper adopts the classical 6T Schmitt trigger circuit structure as shown in Figure 3. Through the interaction of two Schmitt triggers and the design of a positive feedback loop, a stable output signal is achieved. The triangular waveform output at terminal C1 is transformed into a square wave after passing

through the Schmitt trigger circuit. Subsequently, through the Inv1, Inv2, and Inv3 CMOS inverters, the waveform is further shaped and converged. Finally, after passing through the output buffer stage, the signal is output to enhance the circuit's driving capability.

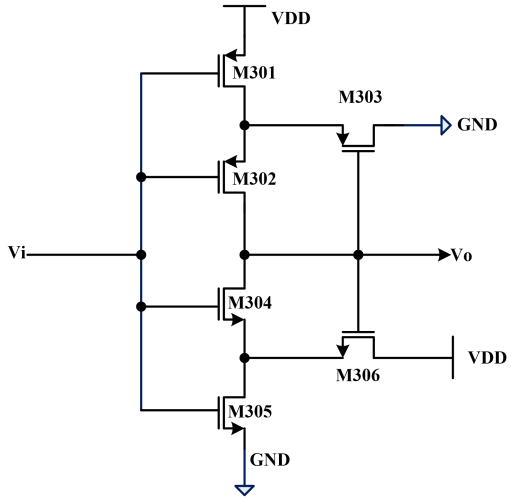


Figure 3. Structure of 6T Schmitt Trigger Circuit

2.2 Bandgap Reference Voltage Generation Circuit Structure

In Figure 2, the control current source Iv is controlled by the input voltage, and the reference current source I0 is controlled by the reference voltage generated by the bandgap reference voltage, which can generate a clock signal with a free frequencyω_0. The bandgap reference voltage generation circuit adopted in this article is shown in Figure 4, which consists of three parts: the start-up circuit, the current mirror circuit, and the bandgap reference circuit. Among them, the operational amplifier in the bandgap reference circuit adopts a seven-transistor differential operational amplifier. After the circuit starts successfully, M209 is turned off; M210-M216 form the current mirror circuit, and it is designed that the current of M211 is equal to the current of M213, and the current of M216 is equal to 10 times the current of M211; the bandgap reference circuit structure adopts the classic circuit structure composed of transistors, resistors and an operational amplifier, and the bias voltage of the operational amplifier is provided by the resistor R4.

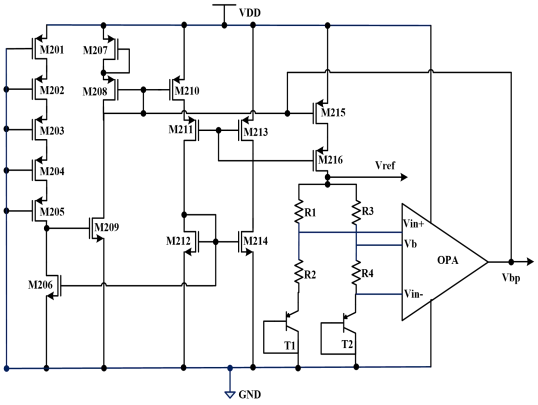


Figure 4. Structure of Bandgap Reference Voltage Generation Circuit

For a bipolar transistor, the base-emitter voltage V_{BE} shows a negative temperature coefficient, and the expression is as Equation (2), V_T = kT/q, for silicon materials, m≈-1.5, and E_g = 1.12 ev.

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)\ V_T - E_g/q}{T} \quad (2)$$

T2 is the transistor with the smallest area, and T1 is composed of n parallel-connected transistors of the smallest area, then the expression of the bandgap reference voltage V_{ref} is as Equation (3).

$$V_{ref} = V_{BE(T1)} + V_T \cdot \ln\left(\frac{nR1}{R3}\right) \cdot \left(1 + \frac{R1}{R2}\right) \quad (3)$$

For the zero temperature coefficient of Vref, there is:

$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{BE(T1)}}{\partial T} + \frac{\partial V_T \cdot \ln\left(\frac{nR1}{R3}\right) \cdot \left(1 + \frac{R1}{R2}\right)}{\partial T} = 0 \quad (4)$$

In this paper, the 180nm process is adopted, V_{BE} = 660 mV, and V_T = 25.6 mV (T = 300K). Substituting into Equation (4), taking n = 8 and R1/R3 = 8, then R1/R2≈4.5. Taking R1 = 24KΩ, then R2≈3KΩ, R3≈5.3KΩ. Taking R4 = R3, the bias voltage Vb of the operational amplifier is approximately 1 V.

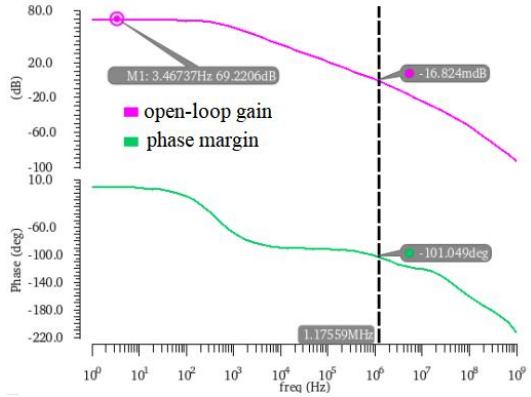
3. Circuit Simulation

Based on the CMSC 180nm BCD process and relying on the design training platform built by our school, MOS devices with a working voltage of 5V are selected to build a simulation circuit to simulate the designed circuit. The simulation verified the good temperature drift characteristics of the output voltage of the bandgap reference voltage generation circuit; the circuit achieved a frequency output of 0.4 MHz-24.27MHz under

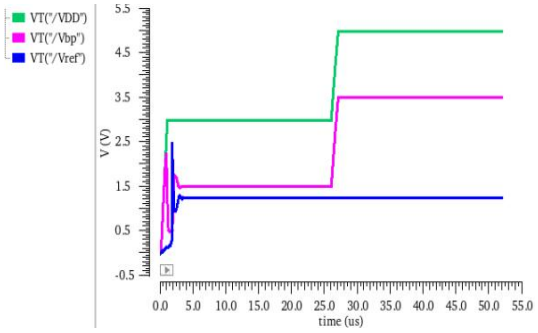
a 5V working power supply and a frequency output of 0.56MHz -13.09MHz under a 3V working power supply; the maximum quiescent current of the circuit under a 5V working power supply is less than 80uA, and the average quiescent current at 10MHz is only 35uA, realizing a low power design. Now the circuit simulation results are introduced.

3.1 Simulation of Bandgap Reference Voltage Generation Circuit

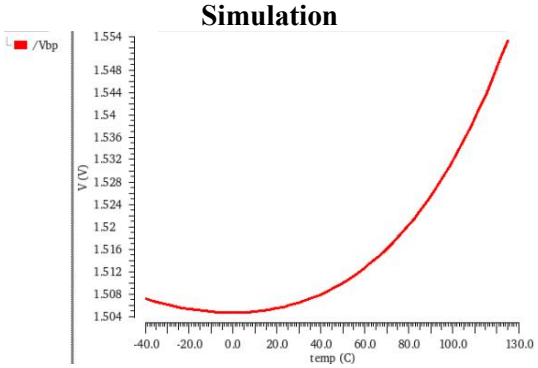
Figure 5 shows the simulation waveforms of the bandgap reference voltage generation circuit. Figure 5(a) is the open-loop gain simulation and phase simulation waveforms of the operational amplifier in Figure 4. The open-loop gain of this operational amplifier at low frequencies is 69.217 dB. The larger the open-loop gain, the higher the negative feedback accuracy and the better the effect; the unity gain bandwidth of the operational amplifier is 1.17 MHz, and the phase margin here is 79°, which meets the requirements of the bandgap reference. Figure 5(b) indicates that under the working voltages of 3V and 5V, Vbp is always 1.5V lower than the power supply voltage, and the Vref voltage value remains unchanged at 1.25V all the time. Under different power supply voltages, Vbp is used as the control voltage of the basic current source. Figure 5(c) and Figure 5(d) respectively represent the temperature curves of Vbp when the temperature is -40°C - 125°C and the power supply voltage is 3V and 5V. It is found that during the entire temperature change process, the change value of Vbp is < 0.05V. Compared with the control voltage and reference voltage of several volts, the influence of temperature on the control voltage of the current source can basically be ignored.



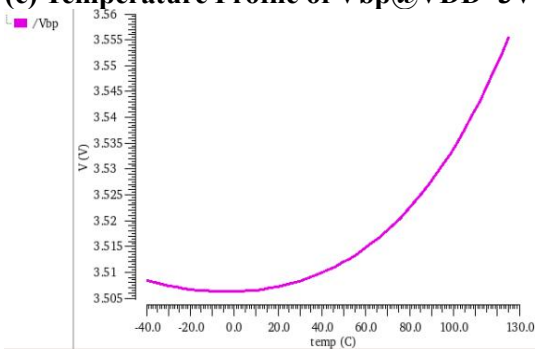
(a) Open-Loop Gain and Phase Margin Waveform of 7-Tube Operational Amplifier



(b) VDD, Vbp and Vref Waveform Simulation



(c) Temperature Profile of Vbp@VDD=3V



(d) Temperature Profile of Vbp@VDD=5V

Figure 5. Simulation Results of Bandgap Reference Voltage Generation Circuit

3.2 Comprehensive Simulation of the Ring VCO Circuit

The Vbp output from the bandgap reference voltage generation circuit is connected to the base current source I0 in Figure 2. The current source is implemented using a series PMOS transistor. During the simulation, the delay capacitor C1 in Figure 2 is realized using an NMOS transistor. For layout design, considering area optimization, a MOM interdigitated capacitor replaces the MOS capacitor to achieve a smaller area. Transient simulations of the VCO circuit were performed with the power supply VDD at both 3V and 5V conditions. The resulting C1 output was a triangular wave, and the final shaped output was a square wave signal. When Vin=0,

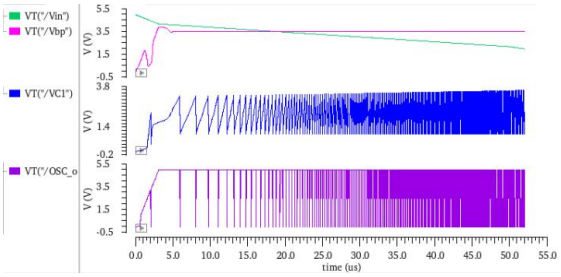
the total current of the voltage controlled current source is at its maximum, the capacitor charging time is at its minimum, and the VCO output square wave frequency is at its highest.

3.2.1 VCO comprehensive simulation @VDD=5V

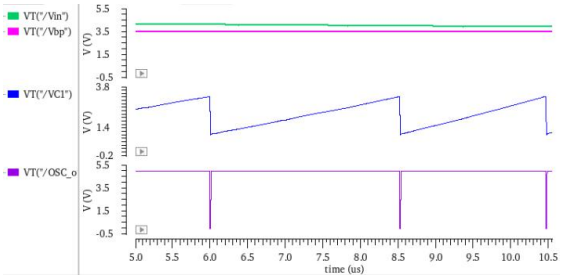
When VDD is 5V, the simulation of the VCO circuit is shown in Figure 6. Figure 6(a) presents the overall waveforms, including the transient waveforms of Vbp, Vin, the triangular wave output of C1, and the output OSC signal. Here, Vbp is 3.5V. During normal operation, Vin linearly varies from 4.2V at 5μs to 2.2V at 50μs. Figure 6(b) shows the magnified waveforms in the 5-10.5μs interval. It can be observed that when Vin is 4.2V, the periods of the triangular wave and the output OSC signal are approximately 2.53μs, corresponding to a clock frequency of 0.4MHz. Figure 6(c) displays the magnified waveforms in the 49.84-50.03μs interval, where Vin is 2.2V, and the periods of the triangular wave and OSC signal are about 0.0836μs, corresponding to a clock frequency of 11.96MHz. Finally, Figure 6(d) illustrates that when Vin is 0V, the periods of the triangular wave and OSC signal are approximately 0.0412μs, corresponding to a clock frequency of about 24.27MHz, as shown in Figure 6(d).

3.2.2 VCO comprehensive simulation @VDD=3V

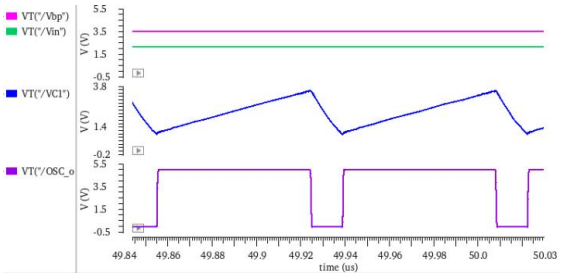
When VDD=3V, the simulation of VCO circuit is shown in Figure 7. Figure 7(a) depicts the overall waveform, presenting the transient waveforms of Vbp, Vin, the triangular wave output of C1, and the output OSC signal. Here, Vbp is 1.5V, and under normal operation, Vin linearly changes from 2.2V at 5us to 0.2V at 50us. Figure 7(b) shows an enlarged view of the 4.7-8.1us interval. It can be observed that Vin is 2.2V, where the periods of the triangular wave and the output OSC signal are approximately 1.77us, corresponding to a clock frequency of 0.56MHz. Figure 7(c) shows an enlarged view of the 49.84-50.03us interval. It can be seen that Vin is 0.2V, where the periods of the triangular wave and the OSC signal are approximately 0.0813us, corresponding to a clock frequency of 12.3MHz. When Vin is 0V, the periods of the triangular wave and the output OSC signal are approximately 0.0764us, corresponding to a clock frequency of 13.09MHz, as shown in Figure 7(d).



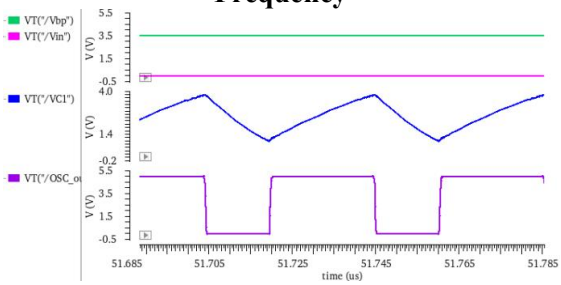
(a) Simulation of the Overall Function of the VCO



(b) VCO Function Simulation@0.4MHz Frequency

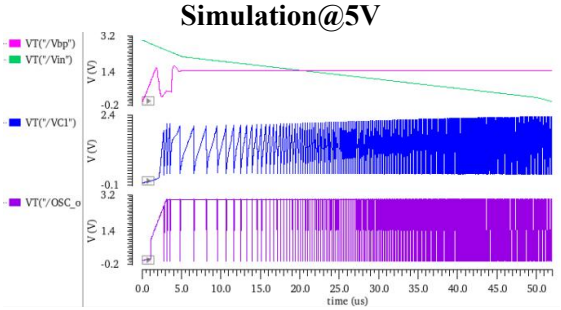


(c) VCO Function Simulation@11.96MHz Frequency

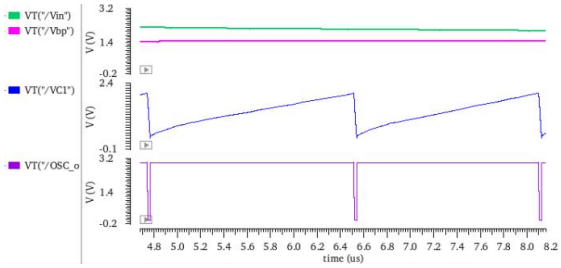


(d) VCO Function Simulation@24.27MHz Frequency

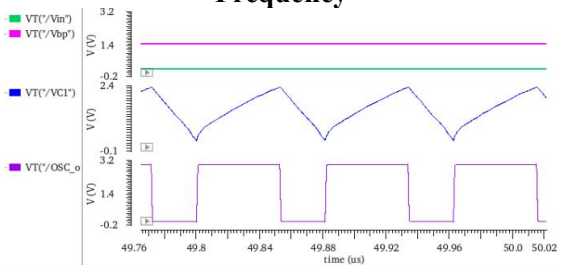
Figure 6. VCO Working Waveform Simulation@5V



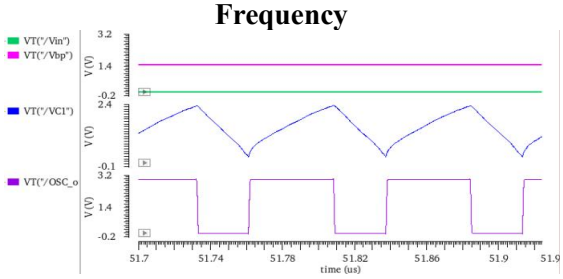
(a) Simulation of the Overall Function of the VCO



(b) VCO Function Simulation@0.56MHz Frequency



(c) VCO Function Simulation@12.3MHz Frequency

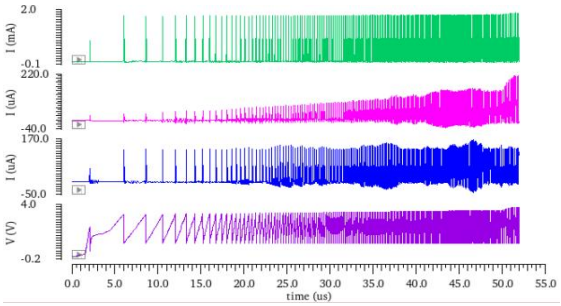


(d) VCO Function Simulation@13.09MHz Frequency

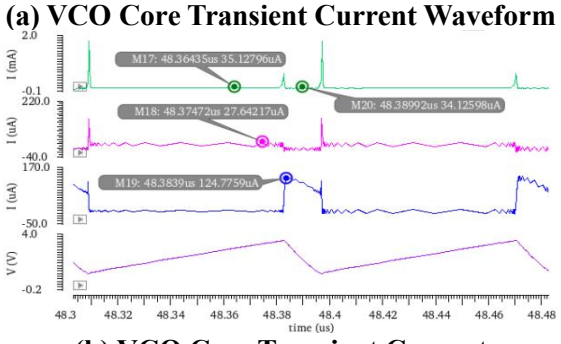
Figure 7. VCO Working Waveform Simulation@3V

3.2.3 VCO operating current simulation

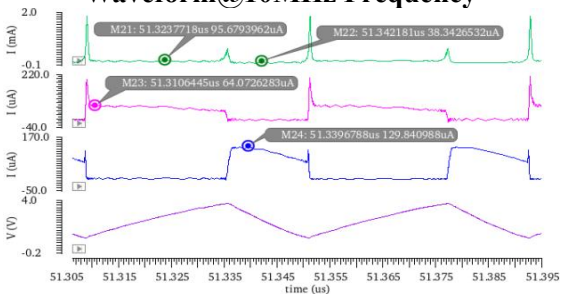
The higher the supply voltage, the greater the power consumption. Therefore, the transient current simulation only considers the case of VDD=5V. Figure 8(a) shows the overall transient current waveform changes. From top to bottom, it displays the VDD supply current waveform of the VCO core circuit, the VCO core charging current waveform, the VCO core discharging current waveform, and the triangular wave output waveform of C1. It can be seen that the overall dynamic current is consistent with the triangular wave frequency. Figure 8(b) shows the transient current waveform under a 10MHz clock condition: the average VDD current is about 35uA, the maximum charging current of the VCO core is 27.6uA, and the maximum discharging current of the VCO core is 124.8uA. Figure 8(c) shows the transient current waveform under a 24.27MHz clock condition when Vin=0: the average VDD current is 73.8uA, the maximum charging current of the VCO core is 64.1uA, and the maximum discharging current of the VCO core is 129.8uA. Similarly, when VDD=3V, the maximum average VDD current is measured to be 22.8uA.



(a) VCO Core Transient Current Waveform



(b) VCO Core Transient Current Waveform@10MHz Frequency



(c) VCO Core Transient Current Waveform@24MHz Frequency

Figure 8. VCO Transient Current Waveform Simulation@5V

Table 1. Performance Metrics Achieved by the VCO Circuit in This Paper

Serial No.	Metrics Name	VDD=5V	VDD=3V	Remarks
1	Control Voltage Range	2.2V-4.2V	0.2V-2.2V	
2	Frequency range	0.4-11.96MHz	0.56-12.3MHz	Within the control voltage range
3	Input-output relation K	5.78MHz/V	5.87MHz/V	Within the control voltage range
4	Max Frequency	24.27MHz	13.09MHz	When the control voltage is 0
5	Maximum average current of VCO circuit power supply	73.8uA	22.8uA	When the control voltage is 0

6	VCO core circuit layout area	0.07*0.04mm^2	
7	Bandgap reference circuit layout area	0.08*0.13mm^2	

3.3 Summary of VCO Performance Metrics

The VCO circuit structure proposed in this paper achieves the performance metrics shown in Table 1. The optimal layout area for the designed circuit is provided through layout design.

4. Conclusion

Based on the CMSC 180nm BCD process, this paper designs a low power, wide-frequency range ring VCO circuit structure for switching power supplies. The circuit structure is simple and easy to implement. By using a voltage controlled current source and a five-stage inverter chain composed of a current-starved ring oscillator, the sensitivity of the VCO frequency to PVT (Process, Voltage, Temperature) variations is reduced. A high-precision bandgap reference is used to provide bias voltage for the basic current source, further reducing the temperature impact on the VCO circuit frequency. Additionally, a Schmitt trigger is used to replace one of the inverters in the chain, improving the VCO circuit's anti-interference capability. The circuit operates at a voltage of 3-5V, with a maximum output frequency of 24MHz, meeting the frequency tunability requirement of 0.4-12.3MHz. The maximum static current is 73.8uA, satisfying the low power requirements for switching power supply chips.

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