Design and Simulation of a 5.8 GHz Gallium Nitride Broadband Power Amplifier Based on ADS and a Double-pi Matching Network

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Abstract: With the development of wireless communication systems, the 5.8 GHz band has become increasingly valuable for applications such as wireless local area networks (WLANs), drone video transmission, and short-range high-speed communication, placing higher demands on the output power, efficiency, and stability of RF power amplifiers.In this paper, a GaN broadband power amplifier operating in the 5.725–5.85 GHz band is designed and simulated using Advanced Design System software. During the design process, GaN power transistors were selected as the core devices, and circuit optimization was achieved through DC simulation, S-parameter stability analysis, load-pull simulation, double-pi matching network design, and harmonic balance simulation.This paper focuses on metrics such as output power, gain, input return loss, and power added efficiency, with the goal of achieving an output power greater than 40 dBm, a power added efficiency greater than 45%, a gain greater than 10 dB, and an input return loss lower than -10 dB. This design can serve as a reference for the simulation and design of 5.8 GHz GaN power amplifiers.

Keywords: GaN Power Amplifier; ADS Simulation; Load-Pull; Double-pi Matching Network; Power Added Efficiency

1. Introduction

RF power amplifiers are critical modules in wireless transmission systems, typically located at the end of the transmit chain. Their primary function is to amplify RF signals to a power level that meets system transmission requirements [1]. The output power, gain, efficiency, and stability of power amplifiers directly affect the transmission distance, energy consumption, and signal quality of wireless communication systems [1,2].In recent years, to further improve transmitter efficiency, high-efficiency architectures such as Doherty power amplifiers have been extensively studied [3]. At the same time, continuous high-efficiency operating modes have provided an important theoretical foundation for the design of broadband, high-efficiency power amplifiers [4]. Furthermore, power amplifiers typically exhibit significant nonlinear distortion under large-signal operating conditions; therefore, behavioral modeling and pre-distortion techniques are also important aspects of modern RF power amplifier research [5].With the development of applications such as wireless local area networks (WLANs), drone image transmission, and short-range high-speed communication, the frequency band around 5.8 GHz holds significant application value in microwave communication systems. Therefore, designing a power amplifier capable of operating near the 5.8 GHz band with high output power and high efficiency holds considerable engineering significance.

Due to their high breakdown voltage, high power density, and good thermal stability, gallium nitride (GaN) devices have been widely adopted in microwave power amplifier design [6]. Compared to traditional silicon-based or gallium arsenide (GaAs) devices, GaN transistors are better suited for high-frequency, high-power applications.However, as the operating frequency increases, issues such as impedance mismatch, potential instability, and the influence of parasitic parameters become more pronounced. These factors can lead to a decrease in the power amplifier's output power and efficiency, and may even cause self-oscillation. Therefore, during the power amplifier design process, comprehensive analysis and optimization of the static operating point, stability, load impedance, and matching network are required.

This paper focuses on the design and simulation

of a 5.725–5.85 GHz GaN broadband power amplifier using the Advanced Design System (ADS). The overall design process includes bias point selection, S-parameter stability analysis, load-pull simulation, double-pi matching network design, bias circuit design, and harmonic balance simulation.Based on issues encountered in previous ADS simulations, this paper emphasizes the need to carefully verify the calculation methods for variables such as output power, DC power dissipation, and power added efficiency during the post-processing stage to avoid unreasonable simulation results caused by errors in port power direction, unit conversion, or DC current extraction. Through this design workflow, this paper aims to provide a clear reference method for the simulation and design of GaN power amplifiers in the 5.8 GHz band.

2. Design Objectives and Simulation Methods

2.1 Design Specifications

The objective of this paper is to design a GaN broadband power amplifier simulation circuit operating in the 5.8 GHz ISM band using Advanced Design System (ADS) software. The target operating frequency range is 5.725–5.85 GHz, a band commonly used in wireless local area networks (WLANs), drone image transmission, short-range high-speed communication, and other ISM band RF systems.Since this band is above 5 GHz, the effects of parasitic parameters, transmission line losses, and impedance matching errors on the power amplifier's performance become more pronounced. Therefore, factors such as device bias, stability, load impedance, matching networks, and bias networks must be comprehensively considered during the design process.

As the core module in the final stage of the RF transmit chain, the primary performance metrics of a power amplifier include output power, gain, power added efficiency, input return loss, and matching network insertion loss [2]. Based on the application requirements of the 5.8 GHz band and the power capabilities of the selected GaN devices, the main design specifications established in this paper are shown in Table 1.

Table 1. Key Performance Metrics

Parameters	Design Objectives
Operating Frequency Band	5.725–5.85 GHz
Center Frequency	5.7875 GHz, approximately 5.8 GHz
Output Power Pout	≥ 40 dBm, i.e., ≥ 10 W
Power Added Efficiency (PAE)	≥ 45%
Power gain	≥ 10 dB
Input return loss S11	≤ -10 dB
Double-pi matching network insertion loss	≤ 0.8 dB
Offset network isolation	≥ 30 dB
Simulation platform	Keysight ADS
Core components	GaN HEMT power transistors

A key design concept of this paper is to adapt the double-pi matching network method, originally applied to the Sub-6 GHz band, for use in the 5.8 GHz ISM band. The double-pi matching network reduces the number of matching network stages while achieving good return loss and low insertion loss over a wide frequency band.Additionally, considering that lumped components are susceptible to parasitic inductance, parasitic capacitance, and packaging effects at high frequencies, the original reference paper also emphasized the necessity of converting some lumped parameters into a microstrip line structure.Building on this foundation, this paper further attempts to implement the matching network using a microstrip approach to reduce the uncertainty caused by the parasitic effects of high-frequency lumped components and to verify the applicability of the double-pi matching network in the 5.725–5.85 GHz frequency band.

2.2 Simulation Platform and Design Process

This paper uses Keysight Advanced Design System (ADS) as the primary simulation platform.ADS is a circuit-level simulation software commonly used in RF, microwave, and high-speed circuit design, capable of supporting DC simulation, S-parameter simulation, load-pull simulation, Smith chart impedance matching, microstrip parameter calculation, and harmonic balance simulation. For the GaN power amplifier studied in this paper, ADS can comprehensively cover the design process from device bias point selection to overall large-signal performance verification.

The overall design process in this paper includes the following steps: First, a suitable GaN HEMT power transistor model is selected, and a DC simulation circuit is established in ADS; second, the static operating point is determined by

scanning the gate voltage and drain voltage to ensure the transistor operates in a Class AB state suitable for power amplification;Next, an S-parameter stability analysis is performed to calculate the stability factor K and the μ factor, thereby assessing whether potential instability issues exist within the target frequency band and a broader frequency range; once stability requirements are met, a load-pull simulation is conducted to determine the optimal load impedance near the target frequency; subsequently, a double-pi output matching network is designed based on the optimal load impedance, and the input matching network and bias network are designed;Finally, the input matching network, transistor, output matching network, and bias circuit are connected to form a complete power amplifier circuit, and harmonic balance simulation and sweep verification are performed [2,6].

3. Device Selection and Bias Point Design

3.1 Selection of GaN Transistors

Currently common materials for RF power devices include Si, GaAs, LDMOS, and GaN. Among these, Si devices are low-cost and have mature processes, but they are limited by breakdown voltage and power density in high-frequency, high-power applications;GaAs devices offer good high-frequency performance but have relatively limited breakdown voltage and thermal performance; LDMOS devices are widely used in low- and mid-frequency power amplifiers, but their gain and efficiency are somewhat limited in frequency bands above 5 GHz.In contrast, GaN HEMT devices offer advantages such as a wide bandgap, high breakdown electric field, high electron mobility, and high power density. They can operate at higher drain voltages and achieve high output power and efficiency in the microwave frequency band [6]. Consequently, GaN HEMTs have become a critical device type in the design of power amplifiers for the C-band and higher frequency bands.

The design objective of this paper is to achieve an output power of no less than 40 dBm within the 5.725–5.85 GHz frequency band. Since 40 dBm corresponds to 10 W of output power, the selected device must possess an RF output capability of at least 10 W. Additionally, to achieve high power added efficiency, the device should feature a high breakdown voltage, low conduction loss, and good thermal stability.Taking these factors into account, this paper selects the commercial GaN HEMT power transistor CGH40010F（Figure 1） as the core amplification device. This device belongs to the 10 W class of GaN HEMTs and is suitable for RF power amplifier designs in the microwave frequency band. Its typical drain operating voltage can be set to 28 V, enabling a large output power swing under high-voltage conditions.

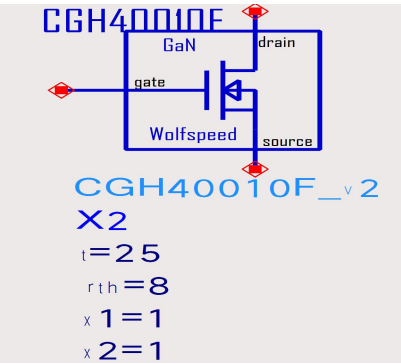

Figure 1. CGH40010F GaN HEMT Device Model in ADS

In the ADS simulation, this paper employs the nonlinear model provided by the device manufacturer for the design. Compared to simple small-signal models, nonlinear models can describe the current, voltage, and power characteristics of the transistor under large-signal operating conditions, making them more suitable for load-pull simulation and harmonic balance simulation of power amplifiers.Since the focus of this study includes metrics such as output power, power added efficiency, and large-signal gain, it is essential to use a nonlinear device model capable of supporting large-signal simulation.

The selection of the CGH40010F is also related to the matching network design objectives of this paper. Since the optimal load impedance of this device near 5.8 GHz is typically not the standard 50 Ω but rather a complex impedance, it is necessary to extract the optimal load point through load-pull simulation and further design the output matching network.This paper employs a double-pi matching network to transform the external 50 Ω load into the optimal load impedance required by the transistor, thereby achieving higher output power and efficiency. There is a close relationship between device selection, bias point setting, and matching network design: the bias point affects the transistor’s large-signal operating state, and the

large-signal operating state, in turn, affects the optimal load impedance obtained via load-pull simulation.Therefore, device selection and DC bias point determination must be completed before proceeding with the matching network design.

3.2 DC Bias Simulation

The DC bias point determines the static operating state of the power transistors and is a critical step in power amplifier design. Different biasing methods cause the power amplifier to operate in different classes, such as Class A, Class AB, Class B, or Class C [2]. The design objective of this paper is to achieve high power added efficiency while ensuring 10 W of output power; therefore, the commonly used Class AB bias method is adopted [2,6]. Class AB power amplifiers can achieve a relative balance between output power, efficiency, and linearity, making them suitable for the 5.8 GHz GaN broadband power amplifier studied in this paper.

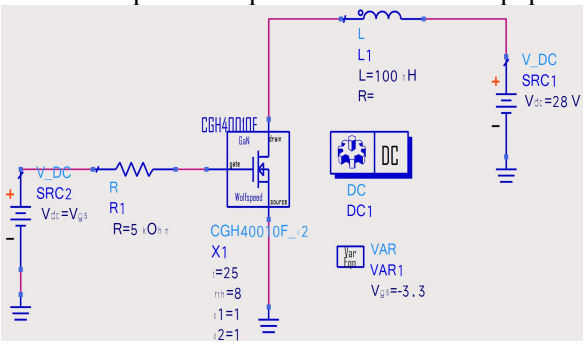

Figure 2. CGH40010F DC-biased Simulation Circuit

When performing DC bias simulation in ADS shown in Figure 2, the primary objective is to determine the appropriate drain voltage V_{DS}, gate voltage V_{GS}, and static drain current I_{DSQ} .Based on the typical operating conditions of the CGH40010F, the drain voltage was initially set to 28 V. A negative gate voltage was applied, and the trend of the drain current as a function of gate voltage was observed through a scanning process. This approach allows for the identification of a suitable static operating point, ensuring that the transistor neither over-conduces nor has its large-signal output capability compromised by excessively low bias. In the DC scan, the drain voltage is fixed at 28 V, and the gate voltage V_{GS} varies within the range of –3.4 V to –3.2 V. The simulation results for the variation of I_D with gate voltage V_{GS} are shown in Figure 3.

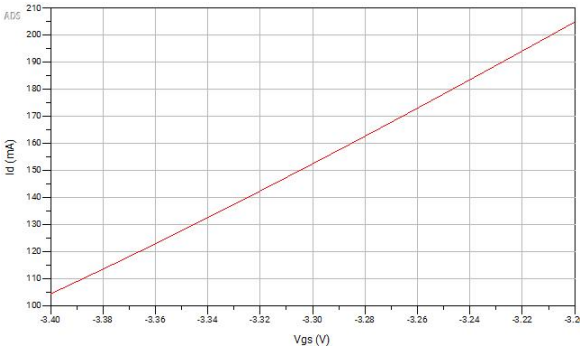

Figure 3. Curve of I_D Versus Gate Voltage V_{GS}

As shown in Figure 3, the drain current gradually increases as V_{GS} rises from -3.4V to -3.2V. When V_{GS}=-3.3V , the drain quiescent current is approximately 152mA. This quiescent current allows the transistor to operate in Class AB mode, while avoiding excessive DC power dissipation caused by an overly high static current. Therefore, this paper ultimately selects V_{DS}=28V, V_{GS}=−3.3V, I_{DQ}≈152mA as the initial bias condition for subsequent stability analysis, load pull simulation, matching network design, and harmonic balancing simulation.

4. Stability Design and Load Impedance Optimization

4.1 S-Parameter Simulation and Stability Analysis

After determining the DC bias point, it is necessary to further analyze the transistor's RF characteristics and stability under small-signal conditions. S-parameter simulation can reflect the device's input reflection, output reflection, forward transmission gain, and reverse isolation characteristics at different frequencies, serving as a crucial foundation for subsequent stability assessment, load pull, and matching network design [2].

Based on the static bias conditions determined earlier, this paper sets up an S-parameter simulation circuit for the CGH40010F in ADS, as shown in Figure 4.In the simulation, the drain voltage is set toV_{DS}=28V , and the gate voltage is set to V_{GS}=−3.3V . The input and output port impedances are both set to 50 Ω. To isolate DC signals and ensure normal RF signal transmission, DC-blocking capacitors are added to the input and output ports, respectively. Additionally, the drain is connected to the DC power supply via a 100 nH inductor to provide drain bias to the transistor.

Furthermore, to improve the transistor's stability near the target frequency band, an RC stabilization network is added at the input in this paper. According to the guidelines on broadband power amplifier design in the references cited earlier, the inclusion of an RC stabilization network at the input requires consideration of its impact on input impedance and gain during subsequent matching network design. Therefore, this section first performs small-signal S-parameter and stability simulations on the circuit with the stabilization network to provide a basis for the subsequent matching network design.

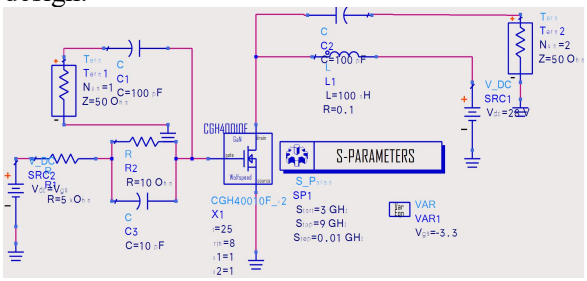

Figure 4. S-parameter Simulation Circuit for the CGH40010F

Figures 5 and 6 show the S-parameter simulation results for the CGH40010F under small-signal conditions, respectively.As shown in Figure 5, at 5.8 GHz, the input reflection coefficient for reverse transmission (S_{11}) is -0.865 dB, and the reverse transmission coefficient (S_{12}) is -35.191 dB. The relatively low value of S_{12} indicates that the transistor possesses good reverse isolation capability, meaning that the feedback from the output signal to the input is weak, which is beneficial for improving circuit stability.

As shown in Figure 6, at 5.8 GHz, the forward transmission gain (S_{21}) is 5.780 dB, and the output reflection coefficient is S_{22} . This indicates that under the current bias and stabilizing network conditions, the transistor still possesses a certain amount of small-signal gain near 5.8 GHz, which can meet the basic requirements for subsequent power amplifier design.However, as shown in the results fromS_{21} and S_{22} , there is still a significant mismatch between the input and output terminals and the 50Ω system impedance, with particularly high reflection at the input. Therefore, input and output matching networks need to be designed to transform the transistor's source impedance and load impedance to appropriate levels, thereby improving power transfer efficiency and output power.

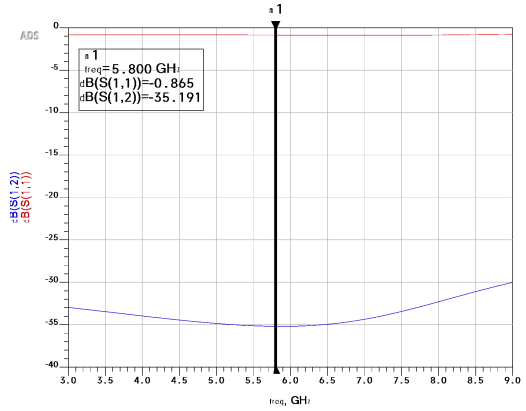

Figure 5. Simulation Results for the Input Reflection Coefficient and Reverse Transmission Coefficient

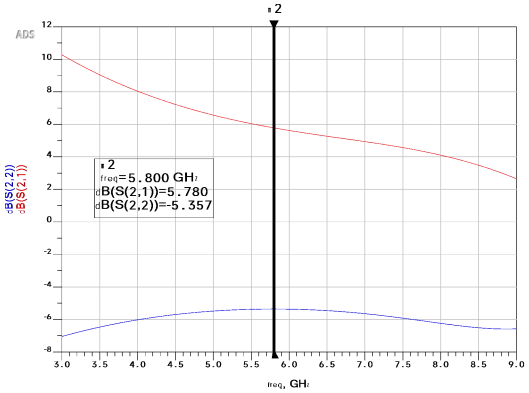

Figure 6. Simulation Results for Forward Transmission Gain and Output Reflection Coefficient

To further assess the circuit's stability, this paper conducted simulation analyses of the stability factor K and |Δ|. For a two-port network, when the stability factor satisfies the condition and |Δ| < 1, the circuit can be considered to be in an unconditionally stable state [2]. The stability simulation results are shown in Figure 7.

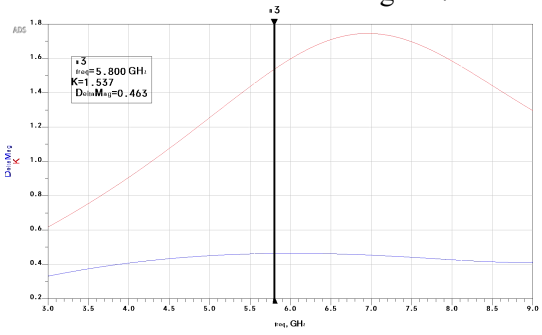

Figure 7. Simulation Results for Stability Factor K and |Δ|

In summary, under the bias conditions of V_{DS}=28V, V_{GS}=−3.3V, the CGH40010F exhibits a certain amount of small-signal gain near 5.8 GHz and demonstrates good reverse isolation performance.After adding the RC stabilization network, the stability factor within the target

frequency band satisfies the stability conditions, indicating that the circuit can operate stably within the 5.725–5.85 GHz operating frequency band. However, since significant impedance mismatches still exist between the input and output, further load-pull analysis is required to determine the optimal source and load impedances, and to design input and output matching networks, in order to achieve high output power and power added efficiency.

4.2 Load-Pull Simulation and Optimal Load Impedance Extraction

After selecting the DC bias point and completing the small-signal stability analysis, it is necessary to further determine the optimal load impedance for the power transistor under large-signal operating conditions.For RF power amplifiers, the output load impedance directly affects output power, efficiency, and the voltage and current swing of the device. Since GaN HEMT devices exhibit significant nonlinear characteristics under large-signal excitation, the load impedance corresponding to their maximum output power is typically not equal to the standard 50 Ω; therefore, a load-pull simulation is required to determine the appropriate load point [2,7].

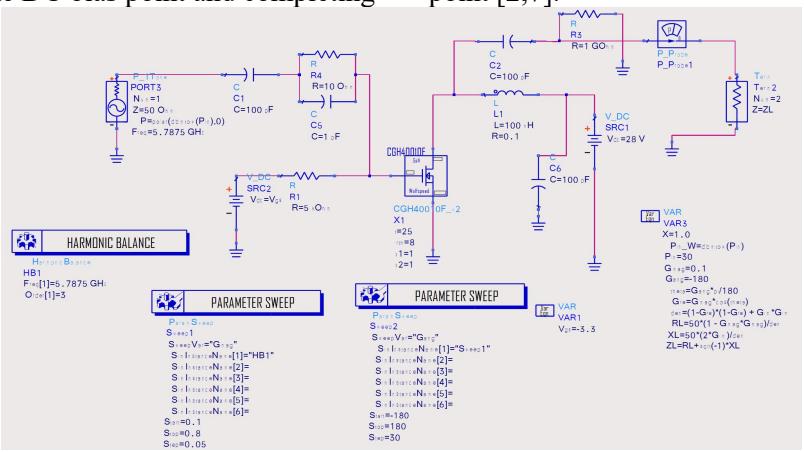

Figure 8. CGH40010F Load Pull Simulation Circuit

Figure 8 shows the CGH40010F load-pull simulation circuit established in ADS.The simulation employs the harmonic balance method, with the operating frequency set to 5.7875 GHz. A single-tone RF signal is applied to the input, and the output is scanned across different load impedance conditions using a variable load. To observe changes in output power under different load conditions, a power probe (P_Probe1) is added at the output, and the output power at the fundamental frequency is measured.

In the load pull simulation, the load state is represented by the reflection coefficient.In this paper, the magnitude of the load reflection coefficient is defined as Gmag, and the phase is defined as Gang. In the ADS schematic, variable equations are used to convert different values of Gmag and Gang into corresponding load impedances, which are then assigned to the output load Term2. Thus, during the parameter sweep, the output load impedance varies with changes in the reflection coefficient, enabling a comparison of output power under different load conditions.

The parameter scan settings are shown in Figure 9. The scan range for the load reflection coefficient magnitude Gmag is 0.1 to 0.8, with a step size of 0.05;the scan range for the load reflection coefficient phase (Gang) is −180° to 180°, with a step size of 30°. This scanning method covers a wide range of load conditions, facilitating the preliminary identification of the load reflection coefficient corresponding to maximum output power.

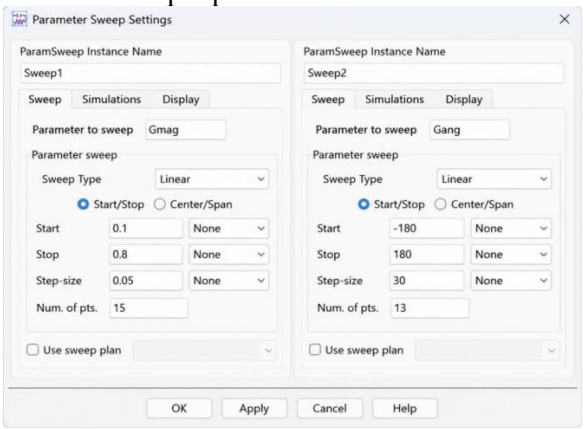

Figure 9. Load Reflection Coefficient Parameter Scan Settings

After the simulation is complete, read the output power of P_Probe1.p at the fundamental

frequency of 5.787 GHz. The scan results show that the output power is at a relatively high level when Gang = −150°. To more intuitively compare power variations near the optimal point, this paper extracts the fundamental output power corresponding to different Gmag values at this phase, as shown in Table 2.

Table 2. Fundamental Output Power Corresponding to Different Gmag Values When Gang = -150°

Gang / °	Gmag	Pout / W
-150	0.400	3.077
-150	0.450	3.186
-150	0.500	3.277
-150	0.550	3.344
-150	0.600	3.378
-150	0.650	3.369
-150	0.700	3.303
-150	0.750	3.161
-150	0.800	2.919

As shown in Table 2, under the condition of Gang = -150°, the output power gradually increases as Gmag increases from 0.400 to 0.600; when Gmag continues to increase to 0.650 and above, the output power begins to decrease. This indicates that, under the current scan conditions, the optimal load point is near Gmag = 0.60.Based on the comprehensive parameter scan results, this paper selects Gmag = 0.60 and Gang = -150° as the optimal load reflection coefficient points for this Load-Pull simulation. At this point, the output power reaches its maximum value of approximately 3.378 W, which converts to approximately 35.29 dBm.It should be noted that the load-pull simulation in this section is mainly used to determine the optimum load impedance at the transistor output reference plane. The output power value of 35.29 dBm is obtained under the specific input excitation, port definition, and load plane used in the load-pull setup. Therefore, this value is not used as the final output power of the complete power amplifier, but only as a reference for the subsequent design of the output matching network.Therefore, the optimal load reflection coefficient can be expressed as: $\Gamma_{l,opt}=0.60\angle-150^{\circ}$. Further conversion to actual load impedance yields $Z_{L,opt}\approx13.34-j12.51\Omega$. This result indicates that at an operating frequency of 5.7875 GHz, the load impedance required for the CGH40010F to achieve maximum output power under the current bias conditions is not 50 Ω, but rather a complex impedance with a low real part and capacitive reactance [7]. This also indicates that if the transistor output is directly connected to a 50 Ω load, power transfer will be suboptimal, and both output power and efficiency will be limited.It should be noted that the load-pull simulation in this section is mainly used to determine the optimum load impedance at the transistor output reference plane. The output power value of 35.29 dBm is obtained under the specific input excitation, port definition, and load plane used in the load-pull setup. Therefore, this value is not used as the final output power of the complete power amplifier, but only as a reference for the subsequent design of the output matching network.

Therefore, in the subsequent output matching network design, this optimal load impedance must be targeted; the matching network should transform the external 50 Ω load into the 13.34−j12.51 Ω required at the transistor output, thereby improving the power amplifier's output power and power added efficiency. These load-pull results provide a crucial basis for the subsequent design of the double-pi output matching network.

5. Matching Network Design and Complete Circuit Design

5.1 Double-pi Matching Network Design

5.1.1 Input matching network

The primary function of a power amplifier's input matching network is to perform impedance transformation between the signal source port and the transistor's input terminal, enabling the input signal to be transmitted as efficiently as possible to the transistor's gate terminal. This reduces input reflections and improves the power amplifier's gain and operational stability.For GaN HEMT devices, the input impedance in the microwave frequency band typically does not match the standard 50 Ω system impedance. Without input matching, significant power reflection occurs at the input, preventing the input power from being effectively delivered to the transistor, which consequently affects the power amplifier's output power, gain, and power added efficiency. Therefore, after completing the static operating point setup and stability analysis, a matching network must be designed for the power amplifier's input.

According to the design objectives of this paper, the power amplifier operates in the 5.725–5.85

GHz frequency band, with the requirement that the input return loss within this band satisfies: $S_{i1} \leq 10dB$. The schematic of the input matching circuit was created in ADS. A 50 Ω port is used as the signal source at the input, and the CGH40010F GaN HEMT device is selected for the transistor.To ensure optimal load conditions at the transistor output during the input matching simulation phase, the output is connected to the best-fit load impedance derived from load pull testing: $Z_{L,opt} \approx 13.34 - j12.51\Omega$. Additionally, the drain bias voltage is set to: $V_{DS}=28V$, and the gate bias voltage is set to: $V_{GS}=3.3V$. Furthermore, an RC stabilization network is added at the transistor gate to improve circuit stability. The input matching network employs a double-pi topology, in which Cin1, Cin2, and Cin3 are parallel ground capacitors, and Lin1 and Lin2 are series inductors. This structure enables flexible broadband impedance matching within the target frequency band [6,8]. The schematic diagram of the input matching circuit is shown in Figure 10.

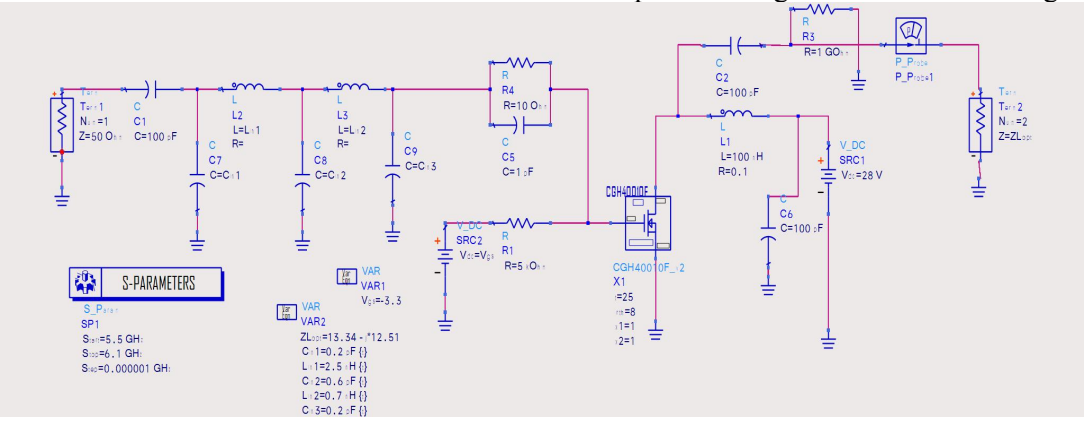

Figure 10. Schematic Diagram of the Input Matching Circuit

During the optimization of the input matching network parameters, the Tune function in ADS was used to jointly adjust the various matching components. The primary optimization objective was to ensure that the input return loss met the requirement of $S_{i1} \leq 10dB$ within the 5.725–5.85 GHz operating band, while simultaneously monitoring changes in the small-signal transmission gain S_{21} to avoid a significant drop in gain during the matching improvement process. After multiple rounds of parameter adjustments and simulation optimization, the final input matching network parameters were determined as shown in Table 3.

Table 3. Input Matching Network Parameters

Parameter	Value
Cin1	0.2 pF
Lin1	2.5 nH
Cin2	0.6 pF
Lin2	0.7 nH
Cin3	0.2 pF

After determining the input matching network parameters, an S-parameter simulation of the circuit was performed. The simulation frequency range was set to 5.5–6.1 GHz, with a focus on observing the changes in the S11 and S21 parameters at the three frequency points of 5.725 GHz, 5.7875 GHz, and 5.85 GHz. The S-parameter simulation results for the input matching circuit are shown in Figure 11.

As shown in Figure 11, at the lower end of the operating band (5.725 GHz), the input return loss (S_{11}) is -11.178 dB; at the center frequency (5.7875 GHz), the S_{11} is -10.8961 dB; and at the upper end of the band (5.85 GHz), the S_{11} is -10.127 dB. S_{11} is less than -10 dB across the entire target frequency band, meeting the input matching design specifications.

At the same time, the S_{21} curve shows that the small-signal transmission gain remains around 9.78–9.82 dB in the 5.725–5.85 GHz band.Specifically, at 5.725 GHz, S_{21} is 9.740 dB; at 5.7875 GHz, S_{21} is 9.7578 dB; and at 5.85 GHz, S_{21} is 9.724 dB. These results indicate that while the input matching network improves input reflection, it does not cause significant gain fluctuations, and the circuit exhibits relatively stable small-signal transmission characteristics within the target frequency band.

In summary, the input double-pi matching network designed in this paper achieves good input impedance matching within the 5.725–5.85 GHz operating band. The input return loss meets the design specification of $S_{11} \leq -10$ dB, while the small-signal transmission gain remains stable.

The parameters of this input matching network can serve as the basis for subsequent output matching design, bias network integration, and joint simulation of the complete power amplifier.

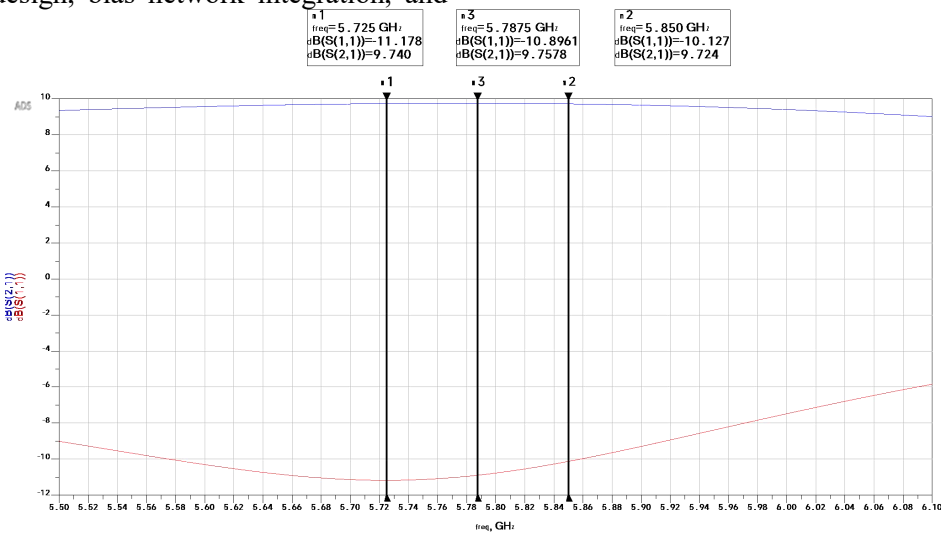

Figure 11. S-parameter Simulation Results for the Input Matching Circuit

5.1.2 Output Matching Network

After completing the design of the power amplifier's input matching network, the output matching network must be designed. The primary function of the output matching network is to match the optimal load impedance required at the transistor's output to the external 50 Ω standard load, thereby improving the power transmission efficiency of the RF signal, reducing output port return loss, and ensuring that the power amplifier exhibits good gain characteristics within the target frequency band.

Based on the load-driven simulation results discussed earlier, the optimal load impedance for the CGH40010F transistor at around 5.8 GHz is: $Z_{L,opt}\approx 13.34-j12.51\Omega$ [7,8]. Therefore, the design objective of the output matching network is to transform the 50 Ω load impedance to a value close to the optimal load impedance, ensuring that the transistor operates under suitable load conditions within its operating frequency range.The structure of the output matching network designed in this paper is shown in Figure 12.

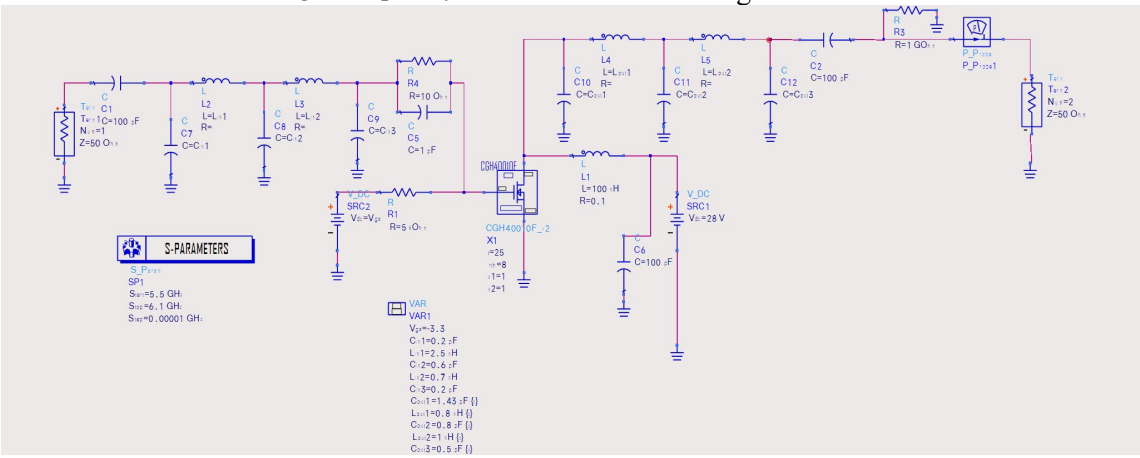

Figure 12. Schematic Diagram of the Output Matching Circuit

To achieve better impedance transformation, the output matching network also adopts a double-pi LC matching structure. This allows for more precise adjustment of the impedance transformation path within the target frequency band, thereby achieving better output matching performance. A DC-blocking capacitor is also added at the output to isolate the drain DC bias from the output port, ensuring that the DC bias network and the RF output network do not interfere with each other.Additionally, the drain bias branch is connected to the DC power supply via an RF choke inductor, ensuring that the DC bias is properly applied to the transistor drain while minimizing RF signal leakage to the power supply. After modeling the output

matching network in ADS, the parameters of each matching component were adjusted using the Tune function.During the tuning process, the primary optimization target was output return loss (S22), while monitoring changes in input return loss (S11) and small-signal gain (S21) to avoid significant adverse effects on input matching and gain flatness resulting from improvements in output matching. After multiple rounds of parameter adjustments, the final component parameters for the output matching network were determined as shown in Table 4.

Table 4. Output Matching Network Component Parameters

Parameter	Value
Cout1	1.43 pF
Lout1	0.8 nH
Cout2	0.8 pF
Lout2	1.0 nH
Cout3	0.5 pF

The S-parameter simulation results of the optimized output matching network are shown in Figure 5-4. To provide a more intuitive analysis of the matching performance, low-frequency, mid-frequency, and high-frequency points within the operating band were selected and marked; the specific simulation results are shown in Figure 13.

As shown in Figure 13, within the operating frequency band of 5.725 GHz to 5.850 GHz, the output return loss (S_{22}) is consistently less than −10 dB, indicating that good impedance matching has been achieved between the output port and the load. At the same time, the input return loss (S_{11}) remains below −10 dB, indicating that the addition of the output matching network has not compromised the input matching performance.The small-signal gain S_{21} is stable at approximately 9.6 dB, with minimal variation across the frequency band, indicating that the power amplifier exhibits a relatively flat gain response within the target frequency band.

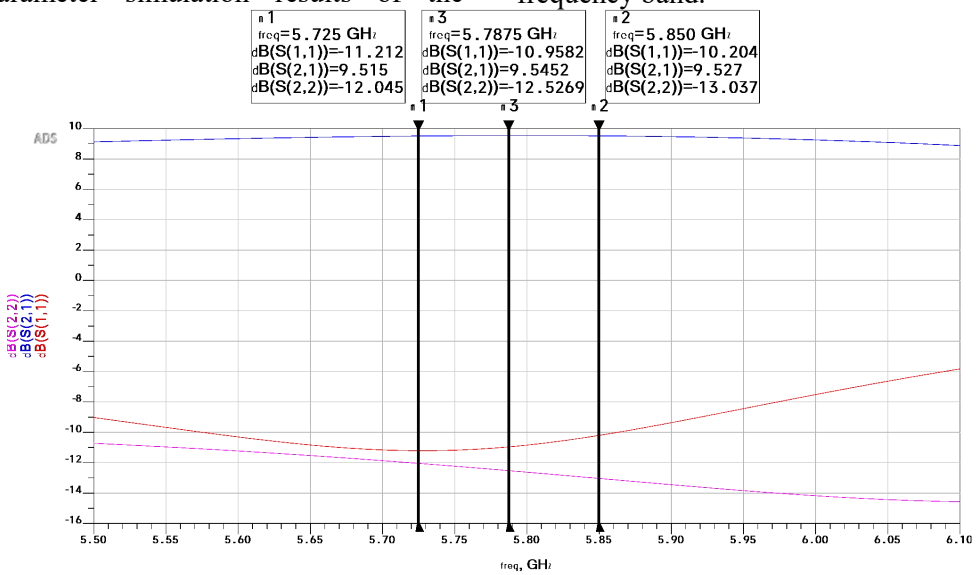

Figure 13. S-parameter Simulation Results of the Output Matching Circuit

In summary, this paper employs a double-pi LC matching structure to complete the design of the power amplifier's output matching network. Simulation results show that this output matching network effectively improves the output matching characteristics within the target frequency band, ensuring that both the input and output return loss of the power amplifier meet design requirements while maintaining a relatively stable small-signal gain. These results provide a solid foundation for subsequent large-signal simulations and power characteristic analysis.

5.2 Verification of the Bias Network

After completing the design of the input and output matching networks, it is necessary to further address the DC power supply for the power transistors. For a power amplifier, the bias network must not only ensure that the devices establish a stable static operating point but also minimize interference with the main RF path. Therefore, following the completion of the matching network design, it is necessary to verify the bias network to demonstrate that it meets the design requirement of "passing DC while blocking RF" and to ensure the reliability of subsequent overall circuit simulations.

The drain bias network designed in this paper is shown in Figure 14. It primarily consists of the RF choke inductor L1, bypass capacitor C6, and DC power supply VDC. The DC power supply is set to 28 V to provide the operating voltage to the transistor drain; inductor L1 is rated at 100 nH and connected in series with the drain supply branch;capacitor C6 is rated at 100 pF and is used for bypass filtering of high-frequency signals. This bias network has a simple structure and effectively achieves isolation between the drain power supply and the RF circuit.

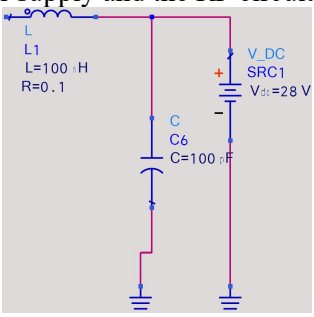

Figure 14: Structure of the Drain Bias Network

From a working principle perspective, inductor L1 has a minimal impact on the drain power supply path under DC conditions, ensuring that the DC voltage is successfully applied to the transistor's drain terminal; whereas at around 5.8 GHz, L1 presents a high impedance to RF signals, effectively suppressing the leakage of high-frequency signals along the bias path to the power supply terminal.At the same time, bypass capacitor C6 exhibits low impedance at high frequencies, effectively bypassing residual high-frequency components from the power supply to ground. This causes the power supply node to approximate ground potential under AC conditions, thereby minimizing the bias network's impact on the main RF channel.Based on the parameters of this bias network, within the target operating frequency band of 5.725–5.85 GHz, the high-frequency impedance of the 100 nH inductor is far greater than the system characteristic impedance of 50 Ω, while the high-frequency impedance of the 100 pF capacitor is far less than 50 Ω.This indicates that the bias network effectively meets the design requirements of "passing DC and blocking RF," demonstrating excellent RF isolation and decoupling capabilities.

In summary, the drain bias network designed in this paper can effectively suppress the leakage of RF signals to the power supply branch while ensuring the normal establishment of the DC operating point of the transistor, and provides good high-frequency decoupling for the power supply side, meeting the design requirements of GaN broadband power amplifiers in the 5.725–5.85 GHz frequency band; therefore, its structure and parameter selection are reasonable.

6. Simulation Results and Performance Analysis

6.1 Small-Signal Simulation Results

To verify the input-output matching characteristics, transmission gain characteristics, and stability of the designed power amplifier within the target frequency band, after completing the design of the input matching network, output matching network, and bias circuit, each component was connected to the power transistor to establish a complete small-signal simulation circuit for the power amplifier. S-parameter and stability simulation analyses were then performed on the ADS platform.The complete circuit consists primarily of an input matching network, a CGH40010F GaN HEMT power transistor, an output matching network, and gate and drain bias networks. The small-signal simulation circuit is shown in Figure 15.

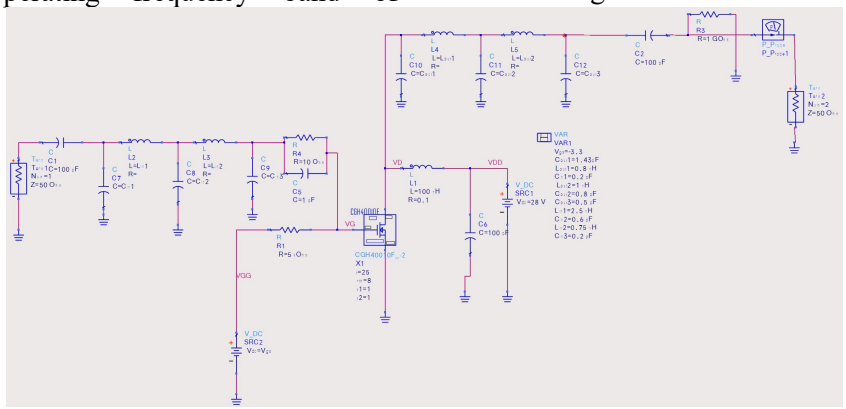

Figure 15. Small-signal Simulation Circuit Diagram of the Complete Power Amplifier

Figure 16 presents the S-parameter simulation results for the complete power amplifier. As shown in the figure, within the target operating frequency band of 5.725–5.85 GHz, the input reflection coefficient (S_{11}) remains at a low level. This indicates that the input matching network effectively transforms the external 50 Ω system impedance to a value close to the impedance required at the transistor input, demonstrating good input matching performance.Combined with the marker data in the figure, it can be further demonstrated that at the lower edge of the band, the center frequency, and the upper edge of the band, the input reflection coefficient (S_{11}) meets the design requirements, indicating that this input matching network possesses good broadband adaptability within the target frequency band.

From the output characteristics, the output reflection coefficient (S_{22}) also remains at a low level within the target frequency band, indicating that the output matching network can effectively achieve load impedance transformation, providing the transistor output with suitable load conditions within the operating frequency band.The simulation results for return loss at both the input and output ends indicate that the designed double-pi matching network still exhibits good matching performance in the 5.8 GHz band, which is consistent with the previous results on load pulling and matching network design.

Regarding transmission characteristics, the forward transmission coefficient (S_{21}) exhibits a generally smooth variation within the target frequency band, indicating that the complete power amplifier possesses a relatively stable small-signal gain response. Although the introduction of the matching network and stabilizing network may affect the device's intrinsic gain to some extent, the simulation results show that the complete circuit maintains good forward amplification capability within the target frequency band, meeting the basic requirements for subsequent large-signal power amplifier design.The reverse transfer coefficient (S_{12}) is generally small, indicating weak feedback from the output to the input. The circuit exhibits good reverse isolation performance, which plays a positive role in reducing the risk of potential oscillation and enhancing circuit stability.

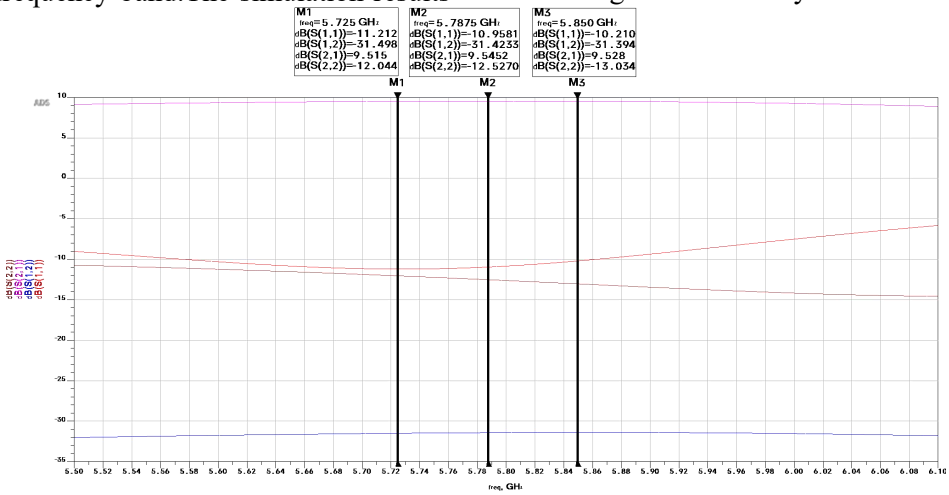

Figure 16. S-parameter Simulation Results of the Complete Power Amplifier

To further verify the stable operation of the complete circuit within the target frequency band, a stability simulation was performed on this power amplifier, with the results shown in Figure 17.As shown in the figure, within the target operating frequency band, the stability criteria consistently satisfy the stability conditions—that is, the stability factor K is greater than 1—while the other stability criteria are also met. This indicates that after incorporating the input matching network, output matching network, and bias network, the complete circuit can still maintain stable operation within the 5.725–5.85 GHz frequency band, with no apparent risk of instability.

Judging from the trend of the stability curve, no sudden changes or critical oscillation points appear within the target frequency band, indicating that the stabilization design measures taken earlier are effective and that the added matching networks have not compromised the device's original stable operating conditions.Combined with the S-parameter simulation results, it can be seen that this

complete power amplifier not only achieves good input-output impedance matching and relatively stable small-signal gain within the target frequency band but also meets the stability requirements for subsequent power amplifier applications, laying the foundation for subsequent harmonic balance simulations as well as output power, power added efficiency, and gain analysis.

In summary, the designed 5.8 GHz GaN power amplifier based on a double-pi matching network exhibits good overall performance under small-signal conditions. Within the 5.725–5.85 GHz operating band, the circuit demonstrates good impedance matching characteristics at both the input and output ports, with a smooth variation in forward transmission gain and good reverse isolation performance, while stability meets the design requirements.It can thus be concluded that this design has a solid foundation for small-signal operation, and further verification of output power, efficiency, and broadband performance under large-signal conditions can be conducted.

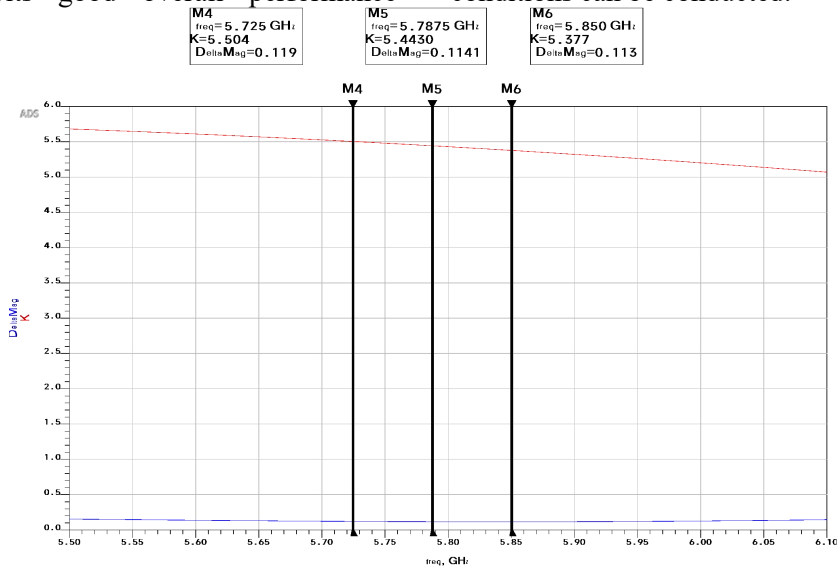

Figure 17. Stability Simulation Results of the Complete Power Amplifier

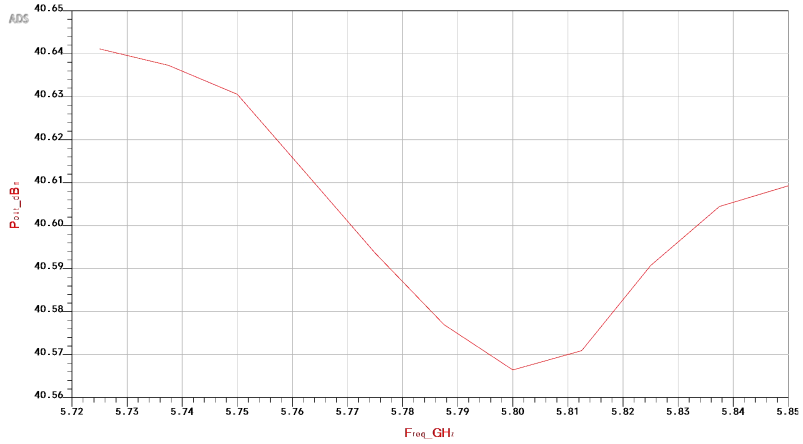

Figure 18. Output power Pout Versus Frequency Curve

6.2 Simulation Results for Large-Signal Harmonic Balance

After completing the design of the input matching network, output matching network, and bias network, this paper performed a large-signal harmonic balance simulation of the complete power amplifier circuit using ADS to verify key performance metrics such as output power, power gain, and power added efficiency within the target frequency band of 5.725–5.85 GHz.In the simulation, the drain bias voltage was set to 28 V, the gate bias voltage was set to -3.3 V as determined earlier, the input power was maintained at 20 dBm, and the fundamental frequency F0 for the harmonic balance simulation was scanned over the 5.725–5.85 GHz range.After simulation, the results of Pout, Gain, and PAE versus frequency were extracted, as shown in Figures 18 to 20.

As shown in Figure 18, within the 5.725–5.85 GHz operating band, the power amplifier's output power generally remains between 40.56 and 40.65 dBm, consistently exceeding the design target of 40 dBm.The output power is approximately 40.64 dBm at the lower end of the frequency range; it decreases slightly as the frequency increases, reaching a minimum of approximately 40.56 dBm near 5.80 GHz, and then gradually recovers at the higher end of the frequency range. The fluctuation in output power is less than 0.1 dB across the entire frequency band, indicating that the power amplifier has a relatively stable output capability within the target operating bandwidth.It should be noted that the output power reported in this section is obtained from the harmonic balance simulation of the complete power amplifier circuit, including the input matching network, output matching network, bias networks, and a 50-ohm load. Different from the load-pull simulation in Section 4.2, this result is measured at the final load port of the complete circuit under the large-signal excitation condition used for overall performance verification. Since the input excitation, measurement reference plane, port definition, and circuit configuration are different, the 40.6 dBm result in this section should not be directly compared with the 35.29 dBm load-pull result in Section 4.2.

As shown in Figure 19, the power gain of the power amplifier within the target frequency band is approximately 20.56–20.65 dB. The trend of the gain curve is essentially consistent with that of the output power curve, also exhibiting a slight dip near 5.80 GHz, but with minimal overall fluctuation.Since the simulation input power is fixed at 20 dBm and the output power is approximately 40.6 dBm, the corresponding power gain is approximately 20.6 dB, which is consistent with the results shown in the figure. The gain throughout the entire frequency band is significantly higher than the design target of 10 dB, indicating that this power amplifier still possesses strong and stable amplification capability under large-signal operating conditions.

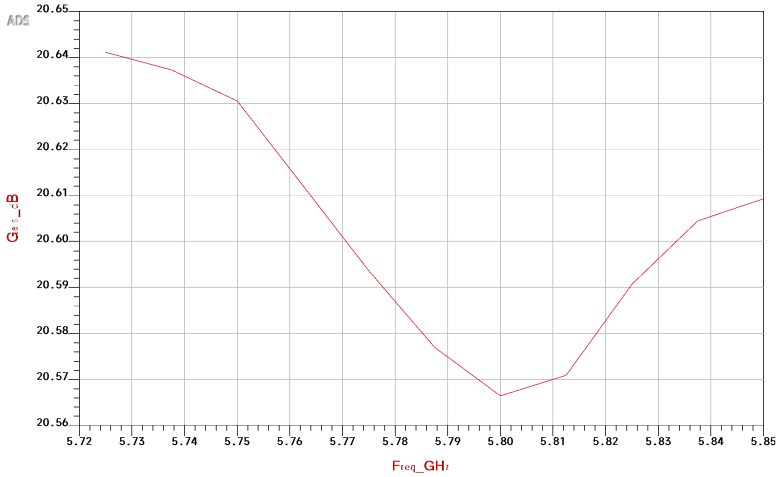

Figure 19. Power Gain vs. Frequency Curve

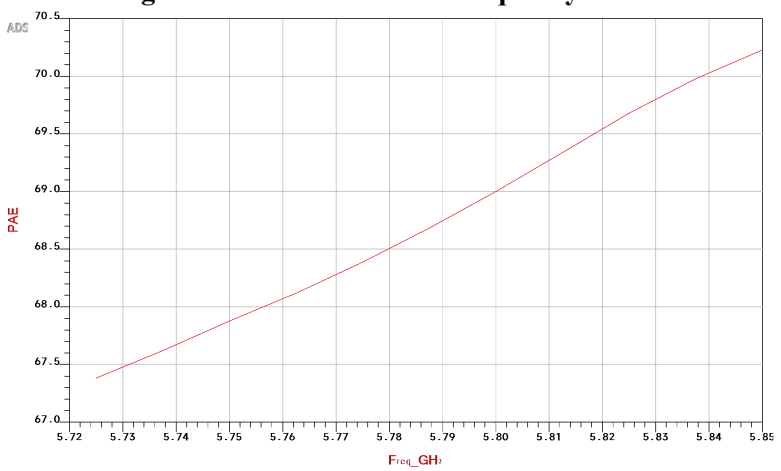

Figure 20. Power Added Efficiency (PAE) vs. Frequency Curve

As shown in Figure 20, within the 5.725–5.85 GHz frequency band, the power added efficiency (PAE) exhibits a gradual upward trend with increasing frequency, rising from approximately 67.4% at the low end to approximately 70.2% at the high end.PAE is significantly higher than the 45% design target across the entire frequency band, indicating that the circuit has high DC-to-RF energy conversion efficiency within the target frequency band. Combining the output power and gain results, it can be seen that this power amplifier achieves high power added efficiency while maintaining high output power and stable gain.

A comprehensive analysis of the simulation results in Figures 18 through 20 reveals that the designed 5.8 GHz GaN broadband power amplifier consistently delivers an output power greater than 40 dBm within the target frequency band, with a stable power gain of approximately 20.6 dB and a power added efficiency maintained above 67%.All three key large-signal performance metrics meet the design requirements, indicating that the designed power amplifier can operate stably within the 5.725–5.85 GHz frequency band and exhibits good broadband output capability and efficiency performance.

7. Conclusion

Based on the Keysight ADS simulation platform, this paper presents the design and simulation of a gallium nitride (GaN) broadband power amplifier operating in the 5.725–5.85 GHz band.The design selected the CGH40010F GaN HEMT as the core device and adopted a Class AB bias configuration. The following steps were sequentially completed: DC bias simulation, S-parameter stability analysis, load-pull simulation, dual π-match network design, bias network verification, and large-signal harmonic balance simulation.Through load-pull simulation, an optimal load impedance near the target frequency was obtained, and based on this, dual π-matching networks for the input and output were designed to ensure good impedance matching and gain characteristics for the power amplifier within the target frequency band.

Simulation results indicate that within the 5.725–5.85 GHz operating band, the designed power amplifier achieves an output power of approximately 40.56–40.65 dBm, a power gain of approximately 20.56–20.65 dB, and a power added efficiency of approximately 67.4%–70.2%, all of which meet the expected design specifications.The results demonstrate that the double-pi matching network adopted in this paper can effectively improve the input-output matching characteristics of the power amplifier, enabling the circuit to achieve stable output performance and high efficiency within the 5.8 GHz band. Overall, the design scheme presented in this paper is feasible and can serve as a reference for the simulation design of 5.8 GHz GaN RF power amplifiers.

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